Date: Fri, 24 Sep 93 04:30:23 PDT
From: Ham-Homebrew Mailing List and Newsgroup <ham-homebrew@ucsd.edu>
Errors-To: Ham-Homebrew-Errors@UCSD.Edu
Reply-To: Ham-Homebrew@UCSD.Edu
Precedence: Bulk
Subject: Ham-Homebrew Digest V93 #54
To: Ham-Homebrew

Ham-Homebrew Digest Fri, 24 Sep 93 Volume 93 : Issue 54

Today's Topics:

Anyone interested in discussing PLL synt (3 msgs)
Ni-Cad charging question
sideband filtering

Send Replies or notes for publication to: <Ham-Homebrew@UCSD.Edu>
Send subscription requests to: <Ham-Homebrew-REQUEST@UCSD.Edu>
Problems you can't solve otherwise to brian@ucsd.edu.

Archives of past issues of the Ham-Homebrew Digest are available
(by FTP only) from UCSD.Edu in directory "mailarchives/ham-homebrew".

We trust that readers are intelligent enough to realize that all text
herein consists of personal comments and does not represent the official
policies or positions of any party. Your mileage may vary. So there.

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Date: 22 Sep 1993 17:52:22 GMT
From: library.ucla.edu!europa.eng.gtefsd.com!howland.reston.ans.net!spool.mu.edu!olivea!koriel!newscast.West.Sun.COM!sunspot!myers@network.ucsd.edu
Subject: Anyone interested in discussing PLL synt
To: ham-homebrew@ucsd.edu

In article 1rg@cc.tut.fi, k23690@lehtori.cc.tut.fi (Kein{nen Paul) writes:
>
>Dana Myers (myers@cypress.West.Sun.COM) wrote:
>
>> Phase noise, for example, would cause the
>> phase comparator to exit the "zero gain" state. The only time the phase
>> comparator is in the "zero gain" state is when both inputs to the loop
>> are in phase and no change is required.
>
>Maybe this is a kind of "cross-over" distortionand it depends how the
>phase detector defines _lock state_. The phase comparator remains
>in "zero gain" (off state) for small phase differences (produced
>by phase noise in the VCO). When the phase difference gets too large,
>the output is suddenly switched to the "linear" state and the loop

>suddenly starts to (over)compensate for the phase difference that
>had accumulated during the "zero gain" state.

The phase detector under discussion (actually a phase/frequency detector) makes decisions based on the rising edges of both inputs.  As a result,  the output of the phase detector, in a locked loop, will be active roughly once every cycle of the reference frequency.  Furthermore, the output of the phase detector has exactly three states; a digital 1, a digital 0, and a high-Z state. When the leading edge of the reference comes before the leading edge of the VCO, the output of the phase detector switches to a digital 1 until the leading edge of the VCO comes.  When the leading edge of the VCO comes before the leading edge of the reference, the phase detector switches to a digital 0 until the reference edge occurs.  When the two signals are both the same, the output is in a high-Z state.

There is no "linear" state; the phase detector simply decides if the VCO needs to increase, decrease or stay the same in frequency.  The phase detector indicates the magnitude of change required by the duration of the output pulses.

This whole notion that the phase detector loses control of the loop is a red herring.  The phase detector is always in control of the loop. If the phase detector does not believe that a change is required in the VCO, then he does his best not to change the VCO by disabling any voltage change to the loop filter.

The sensitivity of the phase detector to small differences in phase, as far as I can tell, is tied to the propagation delay of the phase detector.  In general, the propagation delay is quite small when compared to the average reference frequency.  I'll look at the data book and comment on this later, but I suspect the time it takes the phase detector to make a decision once a phase difference occurs is insignificant when compared the the reference frequency and loop filter bandwidth.

>By injecting a small current, the output is constanly in the linear
>region and it is not constantly jumping in or out between the linear
>state and the off-state.

As I mentioned above, there is no linear state in the output.  It is either "go up in frequency", "go down in frequency" or "don't change".

Any time you inject a current which perturbs the loop, the VCO will require more frequent adjustment and the reference sideband energy will increase. Period.  If injecting current into the loop filter cancels out some undesired bias or leakage current, you may see the sideband energy decrease.  Every time the phase detector output changes from a high-Z state to a 1 or 0, it causes the VCO to change in frequency, which frequency modulates the VCO, which increases the reference sidebands

due to (you guessed it!) frequency modulation.  Causing the phase detector
to make more frequent or larger changes in the VCO will always result in
increased sidebands.

---
 * Dana H. Myers KK6JQ, DoD 466 | Views expressed here are
 *
 * (310) 348-6043 | mine and do not necessarily *
 * Myers@Cypress.West.Sun.Com | reflect those of my employer
 *
 * This Extra supports the abolition of the 13 and 20 WPM tests *

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Date: 23 Sep 93 20:25:40 GMT
From: koriel!newscast.West.Sun.COM!sunspot!myers@RUTGERS.EDU
Subject: Anyone interested in discussing PLL synt
To: ham-homebrew@ucsd.edu

In article 748813130@indirect.com, kg7bk@indirect.com (Cecil Moore) writes:
>Cliff, sounds like a good application for the Techno-Whizzy (DDS).

Since have some Q2220 DDS chips and CA3338E DACs and have built some
T-W style synthesizers, I thought about it myself.

I would suggest that the channelized characteristic of NBFM makes moot
the ability to generate frequencies in between normal "channels", where
a channel in this context means some frequency on a 5KHz spacing (for 2m).

In terms of power consumption and overall size, a PLL synth using a single
chip like the MC145170, which can directly control a VCO up to 170MHz, presents
a number of advantages.  Lower power consumption, less problem with digital
noise getting into the output, much lower cost, much lower power consumption,
etc.

The DDS does offer some advantages; the rapid frequency change is probably
the largest practical advantage.

I ended up deciding a PLL made better overall sense in the application of
generating a base frequency for a multiplying type receiver.

---
 * Dana H. Myers KK6JQ, DoD 466 | Views expressed here are
 *
 * (310) 348-6043 | mine and do not necessarily *
 * Dana.Myers@West.Sun.Com | reflect those of my employer

*
 * This Extra supports the abolition of the 13 and 20 WPM tests *

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Date: 23 Sep 1993 17:30:27 GMT
From: sdd.hp.com!spool.mu.edu!olivea!koriel!newscast.West.Sun.COM!sunspot!
myers@network.ucsd.edu
Subject: Anyone interested in discussing PLL synt
To: ham-homebrew@ucsd.edu

In article 2489@indep1.UUCP, clifto@indep1.UUCP (Cliff Sharp) writes:
>
>   I've thought for a long time about synthesizing my old Sears-su rock-bound
>unit, which has a VFO input.  Sat down and did a little math, and the design
>seems pretty straightforward; oscillators are in the 10-13 MHz range, etc.
>The only problem I foresee is that tuning would require the VCO to change
>frequencies at 833.3 Hz intervals, meaning to me that somewhere in the
>chain, no matter how I design it, I'd end up using an 833.3 Hz frequency
>standard.

Yeah, but not necessarily.

>   That's not hard to produce, even with extreme accuracy; we have a local
>AM station at 1000 KHz that I could phase-lock to for a frequency standard
>and then divide down.  My question is, how effectively is this system going
>to lock and hold a locked condition with such a low frequency as the
>standard?  Seems to me lock would be slow (not good when going from xmit
>to rcv) and not necessarily very stable.

You don't need to phase lock to some external standard; none of my PLL radios do.  The normal approach is to use a crystal oscillator to provide a standard frequency.  The oscillator normally runs in the 6-10 Mhz range; many synthesizer schemes make use of the timebase oscillator as the second local oscillator in a dual-conversion receiver.  The oscillator is divided down to whatever your desired reference frequency is.

This brings us to the reference frequency.  You've selected 833.333 Hz since the normal channel spacing is 10KHz and your radio multiplies the VFO by 12.  However, your radio is limited to generating frequencies at integral multiples of the reference frequency.  This means that using a 10KHz channel spacing will prevent you from operating on frequencies like 147.435, which is an integral multiple of 5KHz.  If you figure it out, this would indicate your 12Mhz synthesizer would use a reference frequency of 416.666 Hz.

Using such a low reference frequency is going to create a real problem in your design with loop lock-up time and (more importantly) reference sideband suppression.  Your loop filter design will need to provide a very high amount

of rejection of the 400 Hz reference present in the phase comp output; practically speaking, you won't be able to realize a good enough loop filter for this. The problem with insufficient reference sideband suppression is that your radio, after mulitplying the VCO by 12, will have birdies every 5KHz on 2m.

A good way to avoid this and still realize your goal is to build a 2m synthesizer. Yup; run a VCO at the desired operating frequency. Then, use a prescaler to divide it by 12. This way, using the Motorola MC145170, you can build a single loop synthesizer which directly generates the required VHF signal using a 5KHz reference and no heterodyne oscillators.

The output of the divide-by-12 circuit would be the VFO input. The radio, I assume,
would phase modulate this without any problem.

As far as frequency stability concerns, you can probably achieve amateur standard stability using a conventional crystal as part of the MC145170 circuit. If you want better, then you can use a TCXO circuit or crystal oven.

I assume you plan to use one VCO to generate both the transmit signal and the receive first local oscillator signal. If so, make sure to add circuitry to the VCO to switch frequency ranges. Also, don't neglect to build and use a lock detect inhibit circuit since you would be experimenting with this and could lose lock by accident.

I would recommend that you verify spectral performance of the synthesizer using a spectrum analyzer before operating on the air, as I recommend whenever building a frequency synthesizer.

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* Myers@Cypress.West.Sun.Com | reflect those of my employer
*
* This Extra supports the abolition of the 13 and 20 WPM tests *


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Date: 22 Sep 1993 19:29:33 -0500
From: library.ucla.edu!europa.eng.gtefsd.com!howland.reston.ans.net!usc!cs.utexas.edu!not-for-mail@network.ucsd.edu
Subject: Ni-Cad charging question
To: ham-homebrew@ucsd.edu

In the magazine Electronics Australia (Oct 91 & Mar 92) there were two articles by James Moxham titled "Longer Life for Ni-Cads"

In the second article he gave a circuit for charging nicads using biased
AC rather than DC.   In this circuit the nicad is alternatively
charged at .1C and discharged at .025C

Does anyone have any comments on my conclusion that I should charge
for 37 hours instead of 14

My reasoning is thus
  Charge duty cycle    50%
  charge current       .1C
  discharge duty cycle  50%
  discharge current    .025C

 effective charge = 50% of .1C  -  50% of .025C
                  = (3/8) of .1C

 therefore charging time should be = (8/3) of 14 hours
                                   = aprox 37 hours

Thanks in anticipation

Graeme Moss
VK3JUD
graemem@acci.com.au

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Date: Thu, 23 Sep 1993 14:57:19 GMT
From: sdd.hp.com!vixen.cso.uiuc.edu!howland.reston.ans.net!spool.mu.edu!olivea!
sgigate!sgi!twilight!odin!chuck.dallas.sgi.com!adams@network.ucsd.edu
Subject: sideband filtering
To: ham-homebrew@ucsd.edu

In article <1993Sep22.165442.29209@kocrsv01.delcoelect.com>,
c2xjcb@kocrsv01.delcoelect.com (James Bach) writes:
|>
|> In article <930921071236@spence>, swilhelm@[128.215.114.181]  (Spence Wilhelm)
writes:
|> > I'm having trouble understanding how superhet recievers filter
|> > out one sideband of a CW singnal.  Is this filtering done by the
|> > IF filter or a function of the BTO?  How does the mechanism work?
|> > I've read the sections about this in the Handbook and RF Design
|> > but neither say much about the subject.  Can anyone shed some light
|> > on this subject?
|> >
|> > --
|> > Spence Wilhelm            KB7TCY         Intel Corporation

```
|> > (602)554-5050                           5000 W Chandler Blvd
|> >
|>
|> What superhet filters-out one of the sidebands?   What sidebands?
|> ====          ===========                         ====
|>
|> (yeah, yeah, I know CW generates sidebands, dependant upon the
|> waveshaping of the xmtr and the code speed, etc., but they are
|> typically so narrow they look like a "spike" on a spectrum analyzer).
|>
|> --
|> James C. Bach              Ph: (317)-451-0455     The views & opinions exp..
|> Advanced Project Engr.     GM-NET: 8-322-0455     herein are mine al...
|> Powertrain Strategy Grp    Amateur Radio: WY9F    NOT endorsed, sponsored,...
|> Delco Electronics Corp.    Just say NO to UNIX!   encouraged by DE or GM.
```

James,

sorry about the filtering on your signature.  trying to keep it to 80 chars across with the News reader additions.  geeez.  IBM 80 column cards are still around, we just do it electronically.  :-)

I think the question here is the following.

Take a superhet receiver and tune across a carrier signal, like
CW with no keying. Why do we loose the signal to one side of the carrier
frequency with a properly aligned receiver with good supression,
i.e. rejection, on the opposite side.  If I may attempt artwork,

```
          *
         * *
        *   *
       *     *
       *     *
       *     *
__________|________   | marks the carrier frequency, f(0)
```

for a properly operating superhet receiver, you get something like

```
           *
           **
           * *
           *  *
           *  *
```

```
           *  *
___________|_________
```

the first graph is the response you get with a DC (direct conversion) receiver and the second is what you get with a SuperHet receiver.

Is the question, why the above response?  Do you want to see the mathematics and description of same?  Someone pick the level of discussion desired.

de chuck k5fo   dit   dit

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Date: Thu, 23 Sep 1993 09:41:44
From: sdd.hp.com!spool.mu.edu!sol.ctr.columbia.edu!news.kei.com!ssd.intel.com!chnews!spence!swilhelm@network.ucsd.edu
To: ham-homebrew@ucsd.edu

References <930921071236@spence>,
<1993Sep22.165442.29209@kocrsv01.delcoelect.com>, <CDtAvJ.93s@odin.corp.sgi.com>e
Reply-To : spence_s_wilhelm@ccm.hf.intel.com
Subject : Re: sideband filtering

In article <CDtAvJ.93s@odin.corp.sgi.com> adams@chuck.dallas.sgi.com (Charles Adams) writes:

```
>stuff deleted
>
>    Take a superhet receiver and tune across a carrier signal, like
>    CW with no keying. Why do we loose the signal to one side of the carrier
>    frequency with a properly aligned receiver with good supression,
>    i.e. rejection, on the opposite side.  If I may attempt artwork,
>
>
>
>              *
>             * *
>            *   *
>           *     *
>           *     *
>           *     *
>    __________|________   | marks the carrier frequency, f(0)
>
>
>    for a properly operating superhet receiver, you get something like
>
>
```

```
>               *
>               **
>               * *
>               *  *
>               *  *
>               *  *
>    ___________|_________
>
>
>    the first graph is the response you get with a DC (direct conversion)
>    receiver and the second is what you get with a SuperHet receiver.
>
>    Is the question, why the above response?  Do you want to see the mathematics
>    and description of same?  Someone pick the level of discussion desired.
>
>    de chuck k5fo   dit   dit
```

Thanks Chuck for helping me get to the heart of my original question.

The question is how does the superhet receiver cut off half of the CW carrier and present information as depicted in your second picture. I understand how IF filtering and BTO mixing can cut off half of the signal when the signal is centered in the IF passband. But, how does it work if the signal is not centered in the IF passband?

Please let me know if there is a good text discussing this subject.


--
Spence Wilhelm           KB7TCY         Intel Corporation
(602)554-5050                           5000 W Chandler Blvd


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End of Ham-Homebrew Digest V93 #54
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